FIG. 1
DIFFERENTIAL SIGNAL OUTPUT CIRCUIT IN FIRST EMBODIMENT

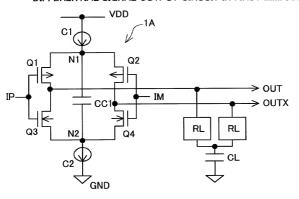
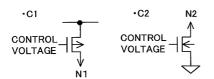


FIG. 2

EXAMPLE OF CURRENT SOURCE IN FIRST EMBODIMENT



SPECIFIC EXAMPLE OF CAPACITOR IN FIRST EMBODIMENT



FIG. 4 SPECIFIC EXAMPLE IN FIRST EMBODIMENT

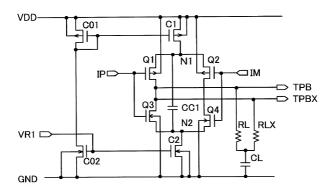


FIG. 5A

DIFFERENTIAL OUTPUT WAVEFORMS ACCORDING TO RESULT OF SIMULATION OF SPECIFIC EXAMPLE OF FIRST EMBODIMENT

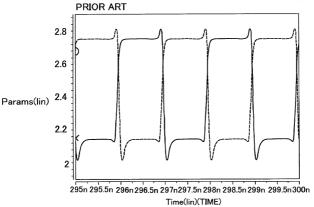
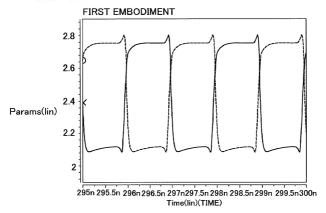


FIG. 5B



The state of the s

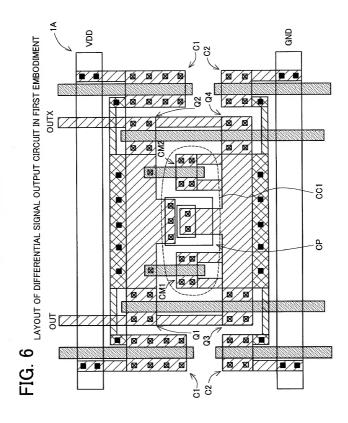


FIG. 7A

DIFFERENTIAL SIGNAL OUTPUT CIRCUIT IN SECOND EMBODIMENT

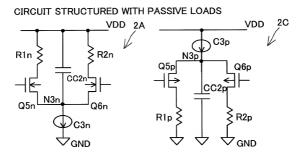


FIG. 7B

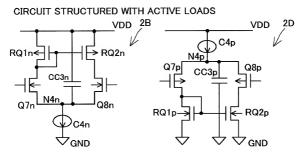
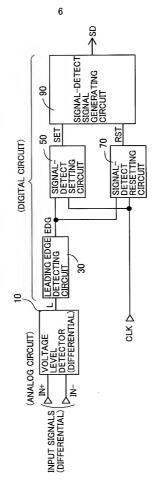
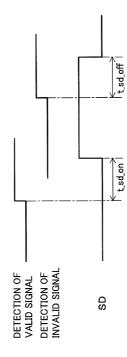


FIG. 8

BLOCK DIAGRAM ILLUSTRATING SIGNAL DETECTION APPARATUS IN THIRD EMBODIMENT



TIMING PARAMETERS OF SIGNAL-DETECT SIGNALS ACCORDING TO P1394b STANDARD



SYMBOL	PARAMETER	TIND	MIN.	UNIT MIN. MAX.
t_sd_on	t_sd_on DELAY TIME FROM DETECTION OF A VALID SIGNAL UNTIL ASSERTION OF A SIGNAL-DETECT SIGNAL	ηsec	ı	901
t_sd_off	t_sd_off DELAY TIME FROM DETECTION OF AN INVALID SIGNAL UNTIL μ sec - NAGATION OF A SIGNAL-DETECT SIGNAL	n sec	_	t_sd_on

FIG. 10 CODE TABLE(1) 8b10bCODES ACCORDING TO P1394b STANDARD

			ODCODES A		O F 13340 31	
	INPUT	ABCDEI FGHJ		INPUT	ABCDEI FGHJ	
NAME	A'B'C'D'E'F'G'H'	RD<0	RD>0	NAME A'B'C'D'E'F'G'H	RD<0	RD>0
	I	DATA_TABLE[I] [0]	DATA_TABLE[I][1]	I	DATA_TABLE[I] [0]	DATA_TABLE[I] [1]
D0.0	00000000	1001110100	0110001011	D4.0 00100000	1101010100	0010101011
D0.4	00000001	1001110010	0110001101	D4.4 00100001	1101010010	0010101101
D0.2	00000010	1001110101	0110000101	D4.2 00100010	1101010101	0010100101
	00000011	1001110110	0110000110	D4.6 00100011	1101010110	0010100110
			0110001001	D4.1 00100100	1101011001	0010101001
D0.1	00000100	1001111001				
D0.5	00000101	1001111010	0110001010	D4.5 00100101	1101011010	0010101010
D0.3	00000110	1001110011	0110001100	D4.3 00100110	1101010011	0010101100
	00000111	1001110001	0110001110	D4.7 00100111	1101010001	0010101110
	00001000	0110110100	1001001011	D20.0 00101000	0010111011	0010110100
D16.4	00001001	0110110010	1001001101	D20.4 00101001	0010111101	0010110010
	00001010	0110110101	1001000101	D20.2 00101010	0010110101	0010110101
D16 6	00001011	0110110110	1001000110	D20.6 00101011	0010110110	0010110110
	00001100	0110111001	1001001001	D20.1 00101100	0010111001	0010111001
	00001101	0110111010	1001001010	D20.5 00101101	0010111010	0010111010
	00001110	0110110011	1001001100	D20.3 00101110	0010111100	0010110011
	00001111	0110110001	1001001110	D20.7 00101111	0010110111	0010110001
	00010000	1110010100	0001101011	D12.0 00110000	0011011011	0011010100
D8.4	00010001	1110010010	0001101101	D12.4 001 10001	0011011101	0011010010
D8.2	00010010	1110010101	0001100101	D12.2 00110010	0011010101	0011010101
D8.6	00010011	1110010110	0001100110	D12.6 00110011	0011010110	0011010110
D8.1	00010100	1110011001	0001101001	ID12.1100110100	0011011001	0011011001
D8.5	00010101	1110011010	0001101010	D12.5 00110101	0011011010	0011011010
D8.3	00010110	1110010011	0001101100	D123 00110110	0011011100	0011010011
00.3				D12.3 00110110 D12.7 00110111		
D8.7	00010111	1110010001	0001101110	D12./ 00 10 1	0011011110	0011010001
	00011000	1100110100	0011001011	D28.0 00111000	0011101011	0011100100
	00011001	1100110010	0011001101	D28.4 00111001	0011101101	0011100010
	00011010	1100110101	0011000101	D28.2 00111010	0011100101	0011100101
	00011011	1100110110	0011000110	D28.6 00111011	0011100110	0011100110
	00011100	1100111001	0011001001	D28.1 00111100	0011101001	0011101001
	00011101	1100111010	0011001010	D28.5 00111101	0011101010	0011101010
D24.3	00011110	1100110011	0011001100	D28.3 00111110	0011101100	0011100011
D24.7	00011111	1100110001	0011001110	D28.7 00111111	0011101110	0011100001
D2.0	01000000	1011010100	0100101011	D6.0 01100000	0110011011	0110010100
D2.4	01000001	1011010010	0100101101	D6.4 01100001	0110011101	0110010010
D2.2	01000010	1011010101	0100100101	D6.2 01100010	0110010101	0110010101
D2.6	01000011	1011010110	0100100110	D6.6 01100011	0110010110	0110010110
	01000100	1011011001	0100101001	D6.1 01100100	0110011001	0110011001
	01000101	1011011010	0100101010	D6.5 01100101	0110011010	0110011010
	01000110	1011010011	0100101100	D6.3 01100110	0110011100	0110010011
	01000111	1011010001	0100101110	D6.7 01100111	0110011110	0110010001
D180	01001000	0100111011	0100110100	D22.0 01101000	0110101011	0110100100
D10.0	01001000	0100111101	0100110010	D22 4 01101001	0110101101	0110100010
D10.4	01001001 01001010		0100110101	D22.4 01101001 D22.2 01101010		
D10.2	01001010	0100110101		D22.2 01101010	0110100101	0110100101
	01001011	0100110110	0100110110	D22.6 01101011	0110100110	0110100110
018.1	01001100	0100111001	0100111001	D22.1 01101100	0110101001	0110101001
D18.5	01001101	0100111010	0100111010	D22.5 01101101	0110101010	0110101010
D18.3	01001110	0100111100	0100110011	D22.3 01101110	0110101100	0110100011
	01001111	0100110111	0100110001	D22.7 01101111	0110101110	0110100001
	01010000	0101011011	0101010100	D14.0 01110000	0111001011	0111000100
	01010001	0101011101	0101010010	D14.4 01110001	0111001101	0111000010
	01010010	0101010101	0)(0)(0)(0)(0)	D14.2 01110010	0111000101	0111000101
	01010011	0101010110	0101010110	D14.6 01110011	0111000110	0111000110
	01010100	0101011001	0101011001	D14.1 01110100	0111001001	0111001001
	01010101	0101011010	0101011010	D14.5 01110101	0111001010	0111001010
N10.3	01010110	0101011100	0101010011	D14.3 01110110	0111001100	0111000011
10.3	01010111	0101011110	0101010001	D14.7 01110111	0111001110	0111001000
D26 A	01011000	0101101011	0101100100	D30.0 011111000		
1026.0	01011001	0101101101	0101100010	D30.4 01111001	0111100100 0111100010	1000011011
020.4	01011001			D30.2 01111010		1000011101
D20.2	01011010 01011011	0101100101	0101100101	D30.Z[U1111010	0111100101	1000010101
D20.0	010111011	0101100110	0101100110	D30.6 01111011	0111100110	1000010110
	01011100	0101101001	0101101001	D30.1 011111100		1000011001
D26.5	01011101		0101101010	D30.5 01111101		1000011010
	01011110		0101100011	D30.3 011111110		1000011100
	01011111		0101100001	D30.7[01111111		1000011110
	10000000		1000101011	D5.0 10100000	1010011011	1010010100
		0111010010	1000101101	D5.4 10100001	1010011101	1010010010
		0111010101	1000100101		<i>Kekki ili kili</i>	TOTOGRADIO
D1.6	10000011	0111010110	1000100110	D5.6 10100011		1010010110

Control of the contro

FIG. 11 CODE TABLE(2)
8b10bCODES ACCORDING TO P1394b STANDARD

	<u> 1 1 4 .</u>		OPCODES A	CCC			
I	NPUT	ABCDEI FGHJ		<u> </u>	INPUT	ABCDEI FGH	
NAME A	B'C'D'E'F'G'H'	RD<0	RD>0	NAME	A'B'C'D'E'F'G'H'	RD<0	RD>0
	1	DATA_TABLE[I] [0]	DATA_TABLE[I] [1]		I	DATA_TABLE[1] [0]	DATA_TABLE[I] [1]
	0000100	0111011001	1000101001	D5.1		1010011001	1010011001
	0000101	0111011010	1000101010			1010011010	1010011010
D1.3 1	0000110	0111010011	1000101100			1010011100	1010010011
D1.7 10	0000111	0111010001	1000101110			1010011110	1010010001
D17.0 1		1000111011	1000110100		10101000	1010101011	1010100100
D17.4 1		1000111101	1000110010	D214	10101001 10101010	1010101101	1010100010
D17.2 1		1000110101 1000110110	1000110101 1000110110		10101011	1010100110	1010100110
017.11		1000111001	1000111001			1010100110	1010100110
D17.5 1		1000111010	1000111010		10101101	11010110110110	MATATOTOTOTO
D17.3 1		1000111100	1000110011			1010101100	1010100011
D17.7 1		1000110111	1000110001	D21.7	10101111	1010101110	1010100001
D9.0 1		1001011011	1001010100		10110000	1011001011	1011000100
	0010001	1001011101	1001010010	D13.4		1011001101	1011000010
	0010010	440340340403	2000101010101			1011000101	1011000101
	0010011	1001010110	1001010110			1011000110	1011000110
	0010100	1001011001	1001011001			1011001001	1011001001
	0010101	1001011010	1001011010			1011001010	1011001010
	0010110	1001011110	1001010011 1001010001			1011001100 1011001110	1011000011 1011001000
D9.7 1	0010111	1001011110 1001101011	1001100100		10111000	1011100100	0100011011
D25.4 1		1001101101	1001100010			1011100010	0100011101
D25.2	0011010	1001100101	1001100101			1011100101	0100010101
D25.6 1		1001100110	1001100110	D29.6	10111011	1011100110	0100010110
	0011100	1001101001	1001101001			1011101001	0100011001
D25.5 1		1001101010	1001101010	D29.5	10111101	1011101010	0100011010
	0011110	1001101100	1001100011			1011100011	0100011100
D25.7 1		1001101110	1001100001	D29.7		1011100001	0100011110
D3.0 1		1100011011	1100010100			1110001011	0001110100
	1000001 1000010	1100011101 1100010101	1100010010 1100010101		11100001 11100010	1110001101 1110000101	0001110010 0001110101
	1000011	1100010110	1100010110		11100011	1110000110	0001110110
	1000100	1100011001	1100011001		11100100	1110001001	0001111001
	1000101	1100011010	1100011010	D7.5	11100101	1110001010	0001111010
	1000110	1100011100	1100010011	D7.3	11100110	1110001100	0001110011
D3.7 1		1100011110	1100010001		11100111	1110001110	0001110001
	1001000	1100101011	1100100100				0001011011
D19.4 1		1100101101	1100100010				0001011101
	1001010	1100100101	1100100101		11101010	1110100101	0001010101
D19.6 1	1001011	1100100110	1100100110	D23.6	11101011	1110100110	0001010110
D19.1 1	1001100	1100101001	1100101001	D23.1	11101100	1110101001	0001011001
D19.5 1	1001101	1100101010	1100101010	D23.5	11101101	1110101010	0001011010
D19.3 1	1001110	1100101100	1100100011		11101110	1110100011	0001011100
D19.7 1		1100101110	1100100001	D23 7	11101111		0001011110
D11.0 1		1101001011	1101000100			0101110100	1010001011
D11.4 1		1101001101	1101000010		11110001	0101110010	1010001101
	1010010	1101000101	1101000101			0101110101	1010000101
D11.6 1		1101000110	1101000110				1010000110
D11.1 1		1101001001	1101001001			0101111001	1010001001
D11.5 1		1101001010	1101001010			0101111010	1010001010
D11.3 1	1010110	1101001100	1101000011	D15.3	11110110	0101110011	1010001100
D11.7 1	1010111	1101001110	1101001000	D15.7	11110111	0101110001	1010001110
D27.0 1		1101100100	0010011011				0101001011
D27.4 1		1101100010	0010011101				0101001101
	1011010	1101100101	0010010101		11111010	1010110101	0101000101
D27.6 1		1101100101	0010010110		11111011		
							0101000110
	1011100	1101101001	0010011001		11111100	1010111001	0101001001
D27.5 1		1101101010	0010011010			1010111010	0101001010
D27.3 1	1011110	1101100011	0010011100	D31.3	11111110	1010110011	0101001100
D27.7 1	1011111	1101100001	0010011110	D31.7	11111111	1010110001	0101001110

SPECIFIC EXAMPLE VOLTAGE LEVEL DETECTOR IN THIRD EMBODIMENT

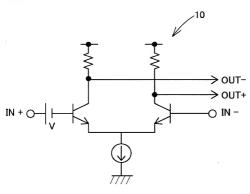


FIG. 13



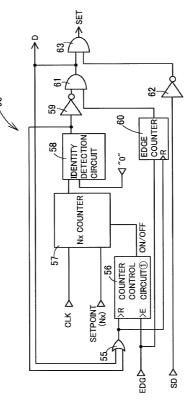


FIG. 14

SPECIFIC EXAMPLE OF SIGNAL-DETECT RESETTING CIRCUIT IN THIRD EMBODIMENT

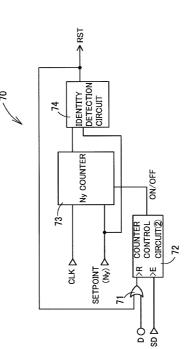


FIG. 15 SIGNAL-DETECT SIGNAL SETTING SEQUENCE

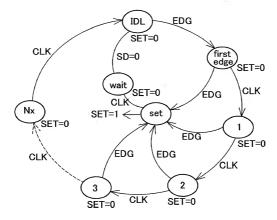


FIG. 16 SIGNAL-DETECT SIGNAL RESETTING SEQUENCE

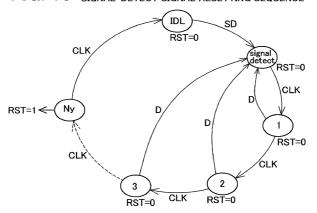


FIG. 17

TIME CHART SHOWING SIGNAL-DETECT SIGNAL SETTING SEQUENCE

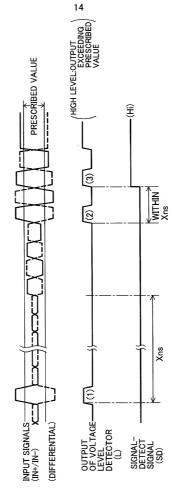


FIG. 18

TIME CHART SHOWING ACTIONS DURING SIGNAL-DETECT SIGNAL SETTING

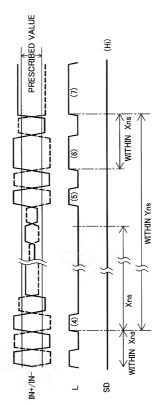


FIG. 19

TIME CHART SHOWING SIGNAL-DETECT SIGNAL RESETTING SEQUENCE

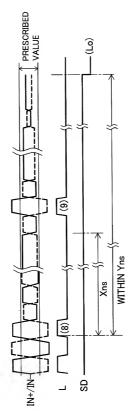


FIG. 20

CONFIGURATIONAL DIAGRAM OF SIGNAL DETECTION APPARATUS IN FOURTH EMBODIMENT

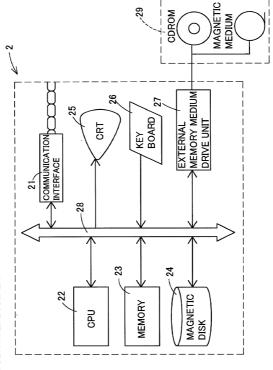
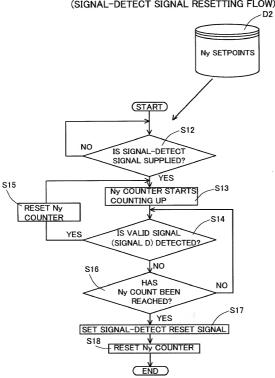


FIG. 21 SIGNAL DETECTION METHOD EXECUTED BY SIGNAL **DETECTION APPARATUS IN FOURTH EMBODIMENT** (SIGNAL-DETECT SIGNAL SETTING FLOW) Nx SETPOINTS PRESCRIBED NUMBER OF TIMES OF EDGE DETECTION (START) S1 **S4** NO IS LEADING EDGE DETECTED? S2 Nx COUNTER YES STARTS INCREASE EDGE COUNT BY 1 COUNTING NO IS Nx COUNTER COUNTING? YES S5 HAS EDGE NO DETECTION REACHED PRESCRIBED **S6** NUMBER OF TIMES? HAS NX NO COUNT BEEN YES REACHED DETECT VALID SIGNAL (SIGNAL D) S12 YES S10 RESET EDGE COUNTER RESET EDGE COUNTER RESET Nx COUNTER -S7 S14 RESET Nx IS SIGNAL-YES COUNTER DETECT SIGNAL SE SET? S9 NO SET SIGNAL-DETECT SET SIGNAL

END

FIG. 22 SIGNAL DETECTION METHOD EXECUTED BY SIGNAL DETECTION APPARATUS IN FOURTH EMBODIMENT (SIGNAL-DETECT SIGNAL RESETTING FLOW)



EXAMPLE OF DIFFERENTIAL SIGNAL TRANSMISSION SYSTEM

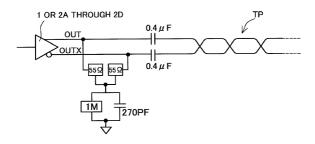


FIG. 24

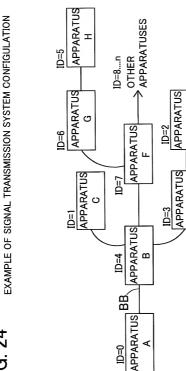


FIG. 25 PRIOR ART

DIFFERENTIAL SIGNAL OUTPUT CIRCUIT ACCORDING TO PRIOR ART

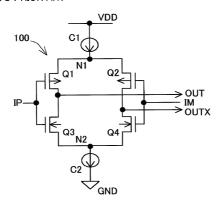


FIG. 26A PRIOR ART

ANOTHER DIFFERENTIAL SIGNAL OUTPUT CIRCUIT ACCORDING TO PRIOR ART

CIRCUIT WITH PASSIVE LOADS

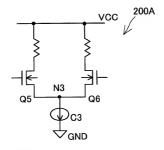


FIG. 26B

CIRCUIT WITH ACTIVE LOADS

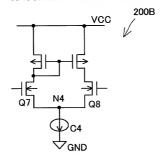


FIG. 27 PRIOR ART

SIGNAL DETECTION APPARATUS ACCORDING TO PRIOR ART

